SIMPLIFYING MIXED-SIGNAL VERIFICATION WITH THE SYMPHONY PLATFORM

SUMIT VISHWAKARMA, PRODUCT MANAGER AMS VERIFICATION,
MENTOR, A SIEMENS BUSINESS

WHITEPAPER

Mentor®
A Siemens Business

AMS DESIGN & VERIFICATION

www.mentor.com

INTRODUCTION

Mixed-signal design is the art of taking real world analog information, such as light, touch, sound, vibration, pressure, or temperature, and bringing it into the digital world for processing. The growth in mixed-signal design has been fueled by an increasing demand for AI, automotive, IoT, communication, and industrial hardware applications (Figure 1).

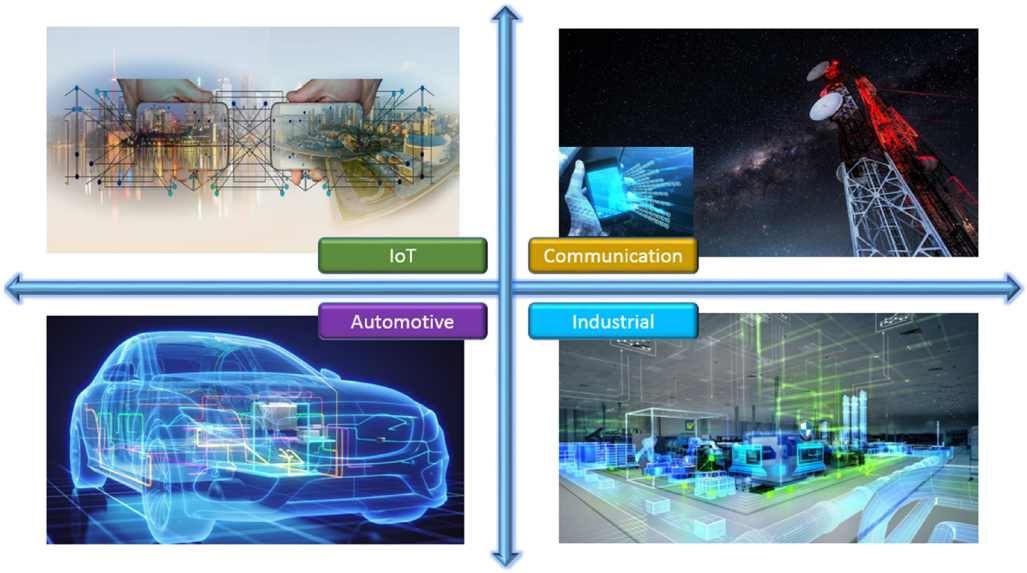

Figure 1: Mixed-Signal market segments.

Designers are finding that these new markets for mixed-signal SoCs are revealing the shortcomings of legacy mixed-signal verification methodologies and tools. Some of these key issues are explored below.

THE "DIVIDE AND CONQUER" APPROACH IS RUNNING OUT OF STEAM

The level of interaction between the analog and digital components in today's mixed-signal SoCs is vastly more complex than it was in the past. The interplay between these domains is so integral to the functionality of the IC that it is no longer adequate to simulate analog and digital subsystems separately in a "divide and conquer" approach. Designers must simulate these two domains together, utilizing an array of advanced mixed-signal verification strategies to obtain the coverage closure required for first pass silicon success.

While designers must simulate the analog and digital subsystems together, the simulation algorithms are fundamentally different. High precision circuits, in many cases, require very accurate SPICE simulation to ensure proper operation, while digital circuits can rely on HDL simulators that run much faster. As a result, the analog simulation will typically dominate the overall system simulation time, as Table 1 explains.

Digital Simulator	Analog Simulator
Digital devices and circuits operate in a discrete domain, where the device pins and circuit nodes have a binary state of either HIGH (1), LOW (0), X (unknown), or Z at any given instant of time.	Analog devices and circuits operate in a continuous domain, where node voltages and branch currents can take arbitrary (positive or negative) values. They vary continuously, as a function of time.
The algorithm solves logical expressions sequentially by triggering events. Simulation is event-driven and discrete-domain based.	Applying Kirchhoff's laws, the algorithm solves the entire analog system matrix at every time step.
There is a defined signal flow from input to output.	There is no defined signal flow in any direction and circuit elements can instantaneously influence any other element in the matrix.

Table: 1 Digital solver versus analog solver.

THE UNSTRUCTURED VERIFICATION FLOW IS NOT ADEQUATE

The digital verification flow is structured and follows an automated design methodology, while analog verification typically does not. But, a transition to a structured analog flow, that is more efficient and allows designers to handle the growing size of analog and mixed-signal circuits, is clearly needed. In digital design, the metric-driven verification approach helps engineers achieve desired coverage closure.

The need for more comprehensive verification of mixed-signal SoCs means analog verification teams must go beyond traditional approaches like directed tests, sweeps, corners, and Monte Carlo analysis. Teams need to adopt digital verification techniques to enable regression testing of mixed-signal SoCs. These techniques include: automated stimulus generation, coverage, and assertion-driven verification combined with low-power verification.

STRINGENT SAFETY AND RELIABILITY STANDARDS REQUIRE NEW APPROACHES

Stringent specifications and standards, such as those defined by ISO 26262, place growing pressure on verification teams to achieve adequate verification coverage for their mixed-signal SoCs. Analog and digital blocks in these ICs are interlaced and subject to process variations that increasingly affect circuit performance. To address these challenges, verification teams need to run an increasing number of mixed-signal simulations at both the top level and the sub-system level. These mixed-signal simulations need to be fast, accurate, easy to setup, and debug, and seamlessly integrate into existing analog and digital verification flows.

MIXED-SIGNAL VERIFICATION OWNERSHIP IS REQUIRED

Successful verification of a mixed-signal SoC requires experts from various disciplines working in concert towards a common goal. As organizations transition towards a top-down, mixed-signal verification methodology, there is often confusion about the ownership of the project. Within the mixed-signal design team, there are a number of individuals fulfilling leadership roles and responsibilities (Figure 2) that are necessary to assure the success of the entire SoC:

- Block Designer: responsible for one or more design blocks within that project that takes care of all aspects of implementation of that block. There are digital block designers and analog block designers.
- Modeling Engineer: develops the sophisticated models used by other members of the team. For simple blocks, block designers can create their own models using their knowledge of the block design and specification. For more complex blocks, like a phase-locked loop (PLL) or a clock-and-data recovery (CDR) circuit, the behavioral models are often created by a Modeling Engineer and they require specialized modeling skills and experience.

- System Integrator: is primarily responsible for specifying how the various blocks that make up a design are assembled. The System Integrator is responsible for the top-level verification and owns the task of developing the overall testbench.

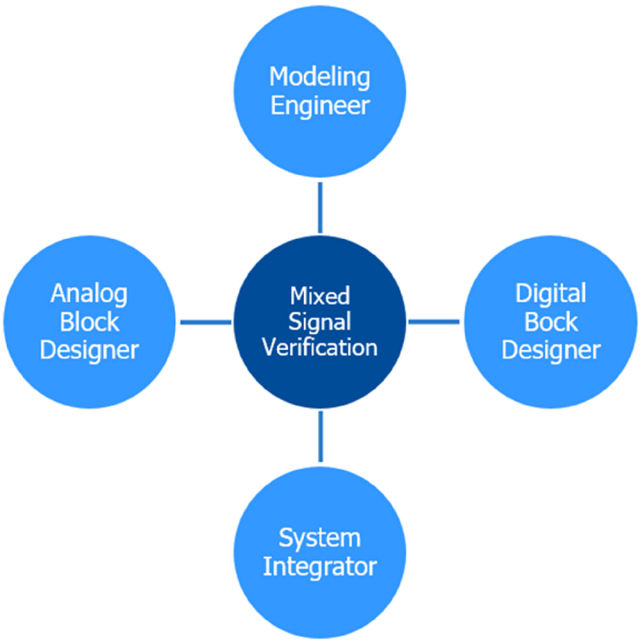

Fig 2: Mixed-Signal design and verification owners.

Because there are so many different disciplines and roles, a mixed-signal tool must be easy-to-setup and use for debug, and it must seamlessly integrate into existing analog and digital verification flows so that any member of the team can identify bugs at any stage of design cycle.

UNDERSTANDING MIXED-SIGNAL METHODOLOGIES

Mixed-signal design plays a critical role in ICs that have high-performance, low-noise analog interfaces connected to large digital signal processing blocks. This is the case in networking and wireless communication applications, where an analog/RF signal is converted to digital, processed, and converted back to analog. Mixed-signal design is now a key requirement for wearable, IoT, and automotive applications and the number of periphery sensors is growing in these applications. Sensors are proliferating to the periphery of individual blocks and they will eventually propagate to the periphery of the SoC itself. The various parts of the circuit must communicate more quickly in order to meet the increasing performance requirements for the overall system. In AI chips, for example, communication between processors and between memory and processors occurs at hundreds of gigabytes per second.

The combination of growing design size, dramatic changes in analog-digital integration and complexity, and the variability introduced at advanced process nodes threatens mixed-signal chip yield, performance, and longevity. As a result, mixed-signal methodology has evolved continuously over the years to address these challenges. The two primary design methodologies are “analog driven” bottom-up and “digital driven” top-down.

ANALOG DRIVEN METHODOLOGY

Analog designers are familiar with the bottom-up approach, where the design process starts with the design of individual blocks that are then combined to form the system. The design of a block starts with a set of

specifications and ends with a transistor-level implementation. Each block is verified as a stand-alone unit against specifications and then combined and verified together. Designers have the necessary understanding of the desired block functionality and they can focus on the initial product delivery, allowing work to begin immediately on critical portions of the system. However, in this flow, system-level design errors do not surface until late in the design cycle and might require costly design iterations.

The development of behavioral models (Figure 3) happens late in design cycle, when transistor-level simulations take too long to run. This begins to happen when designers integrate multiple SPICE blocks together. The amount of time and effort needed to create accurate models may push the project off schedule and model quality could be compromised.

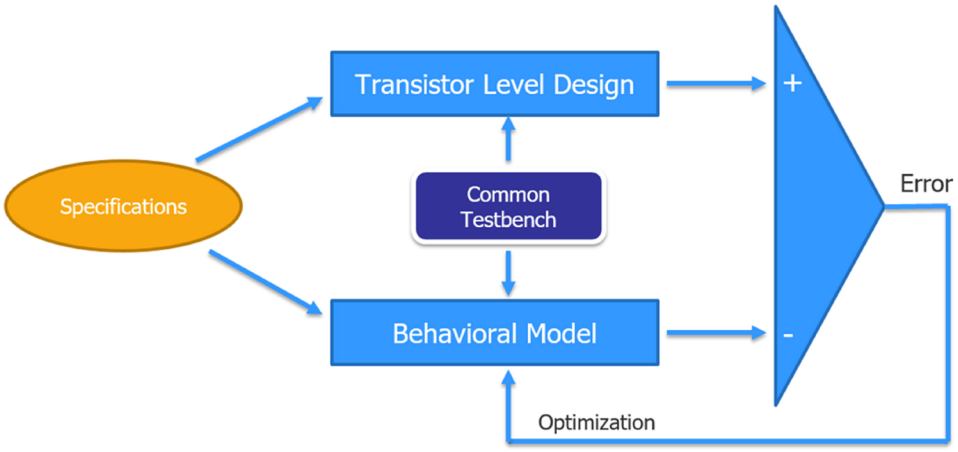

Figure 3: Behavioral model validation using optimization.

After the model matures, it is easy to make minor tweaks to customize it for new specifications on the next version of the design. While turn-around time for project completion in an analog centric approach depends heavily on SPICE simulator performance, accurate modeling using Real Number Model (RNM) has recently seen good traction to expedite verification cycles.

DIGITAL DRIVEN METHODOLOGY

Digital designers and verification engineers rely on a top-down methodology which is a *planned* approach that effectively integrates modeling into the system/SoC development process. This approach primarily relies on discrete time behavioral models of a subsystem that result in faster functional verification (100x to 1000x faster) than transistor-level verification.

The top-down design approach results in higher confidence that the completed design will meet the original schedule and system specifications. The design team can reuse and re-verify alternative designs, packages, or implementations without having to rebuild a new context or verification infrastructure.

With this approach, however, a system-level description is needed that involves knowledge of the system and system-level descriptive language(s) or tool(s). Additionally, a full system-level testbench is needed from the start of the verification process. For the digital driven methodology, the behavior of the analog blocks is an approximation, a mathematical representation of functionality that might not reflect the actual physical silicon effects.

A good engineering methodology uses a "meet-in-the-middle" approach which is a balance between top-down and bottom-up. In an organization, design groups can pick one approach over another based on their technical expertise, project schedule, and the scope of the project.

MODERN MIXED-SIGNAL VERIFICATION CHALLENGES

As design complexity multiplies, verification complexity explodes. Verification is now the art of applying many unique methodologies for each class of sub-design within an IC. In the pure digital verification space, the advent of new technologies, such as constrained-random data generation, assertion-based verification, coverage-driven verification, formal model checking, and intelligent testbench automation, have changed the way teams achieve functional verification productivity. However, most of these advances and new technologies have not been perfected for the analog domain and have not been extended to verify mixed-signal designs (Figure 4).

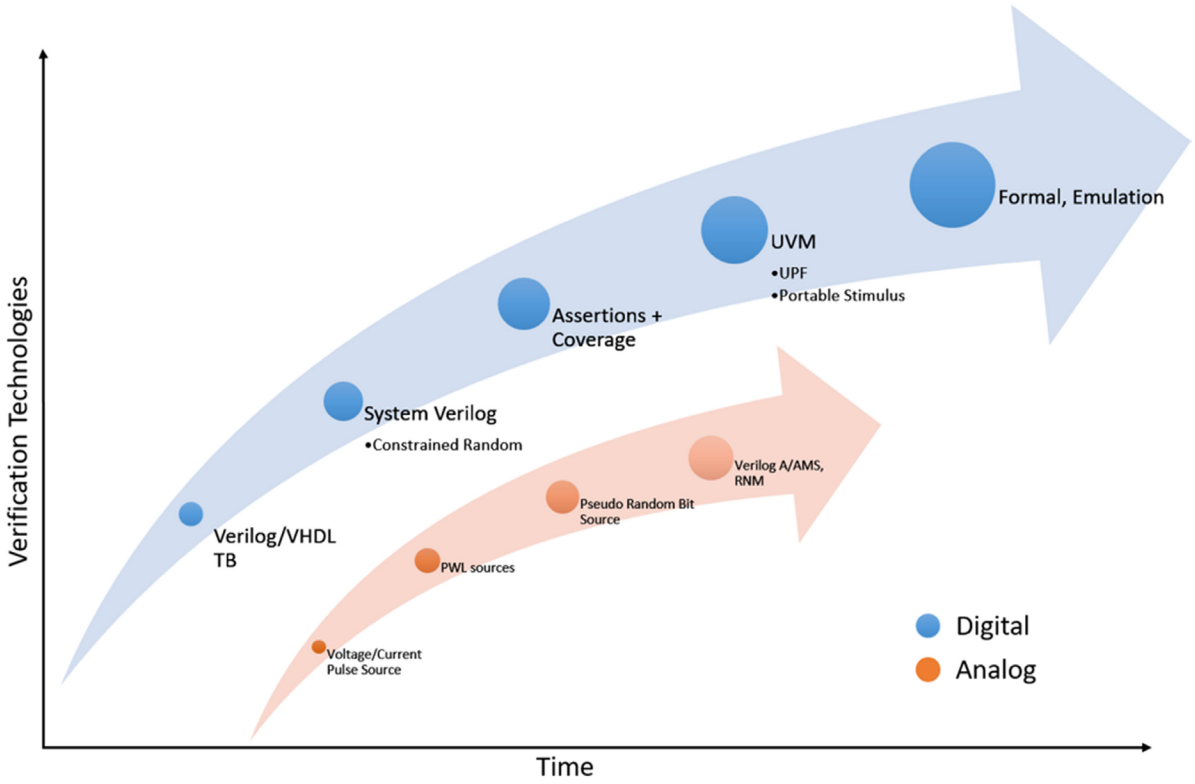

Figure 4: Digital versus analog/mixed-signal verification technology progression.

Mixed-signal verification is evolving at a slower pace and it faces some key challenges which are explored below.

PERFORMANCE

Simulating the behavior of a mixed-signal design requires both digital and analog solvers to work in parallel and in a synchronized fashion. In mixed-signal simulation, analog solvers become the bottleneck in meeting the overall performance goal for verification. To achieve reasonable simulation speeds, many mixed-signal teams employ analog behavioral modeling. However models are becoming more difficult to develop, integrate, and utilize effectively at smaller technology nodes (like 10/7nm) as design complexity, process variation, and physical effects add to the number of variables that need to be taken into account.

Teams face a key question: how much time should the team invest in creating models and is the return on investment worth the resources and time spent? For complex analog designs at smaller technology nodes, design teams still prefer to use a SPICE simulator which guarantees accuracy. This puts immense pressure on the EDA tool provider to offer a solution that can satisfy both performance and accuracy requirements that design teams demand.

MULTIPLE ENGINE AND DESIGN ENVIRONMENT

There is no single methodology for verifying a SoC. Teams employ multiple simulation engines in different contexts through varying verification flows. The design verification methodology changes from low-level design up to the system level. Migrating designs between engines can take months and a tremendous amount of effort. Additionally, the cost of migrating a SoC verification flow grows exponentially with design size.

Digital and analog teams working on a common SoC engage in multiple activities that involve different tools without any means of effective communication between them. It gets challenging when the time comes to integrate the IC for full mixed-signal verification because no designer has complete insight into the use models and configurations of all the tools in the flow. What is needed is a platform that can easily fit into any design environment and verification methodology for efficient verification closure.

COMPLEX USE MODEL

Traditionally, analog and digital designers work in different, often disjointed, design environments. While an analog designer focuses on optimizing design performance (for example, improving gain, bandwidth, and SNR), the digital engineer is working to improve coverage. Often, specification changes and design ECOs result in the addition/removal of simulator commands and options. Both designers eventually bring their designs together to run through the final mixed-signal verification flow. The mixed-signal tool should be adaptive to any changes in the individual analog or digital simulator options, otherwise the hand-off of the design from either the analog or digital designer to the System Integrator becomes harder, which negatively impacts productivity.

MIXED-SIGNAL DEBUG

In mixed-signal design, errors most often occur at the interfaces between analog and digital blocks. Frequently, bugs in the interfaces are identifiable only at a higher level of hierarchy, sometimes at the I/O pins (Figure 5).

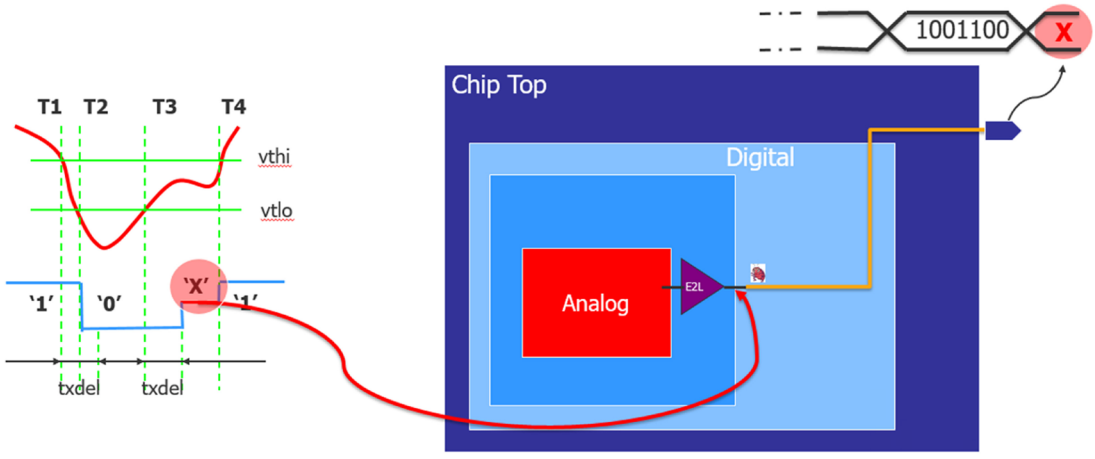

Figure 5: Mixed-Signal bugs.

Mixed-signal debug gets even more complicated when the design employs advanced, low-power techniques. For example, data corruption in a digital block due to faulty power sequencing can pass to an analog block, resulting in erroneous voltage conversion. Scenarios like this are difficult to debug by analog designers who are unaware of digital low-power techniques.

INTRODUCING SYMPHONY

The next-generation Symphony Mixed-Signal Platform provides designers with unprecedented flexibility for choosing their own design methodology: bottom-up, top-down, or any combination of the two**.** Designers can make intelligent trade-offs by choosing detailed, continuous analog models or SPICE for high accuracy and discrete behavioral models for simulation speed performance.

Symphony Mixed-Signal Platform is the industry's fastest and most configurable mixed-signal solution to accurately verify design functionality, connectivity, and performance across analog/digital (A/D) interfaces at all levels of the design hierarchy for all IC applications (Figure 6).

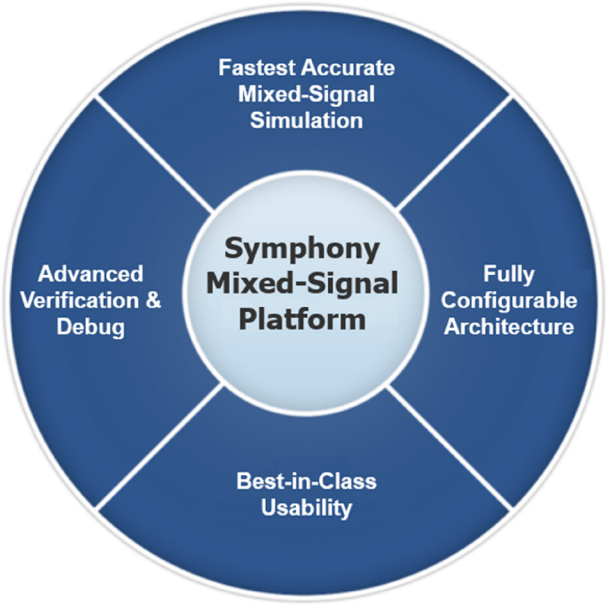

Figure 6: Symphony Mixed-Signal Platform.

ACCURACY AND SPEED ADVANTAGE

Symphony's modular architecture leverages Mentor's Analog FastSPICE (AFS) circuit simulator to provide fast mixed-signal simulation performance with nanometer (nm) SPICE accuracy and capacity of 20M SPICE elements. With certified accuracy by the world's leading foundries, AFS delivers 5–10x faster performance than traditional SPICE and 2–6x faster performance than parallel SPICE simulators. Symphony has been proven on a wide range of ICs and IC subsystems including ADCs, SerDes, PLL, Oscillators, and sensors (Figure 7).

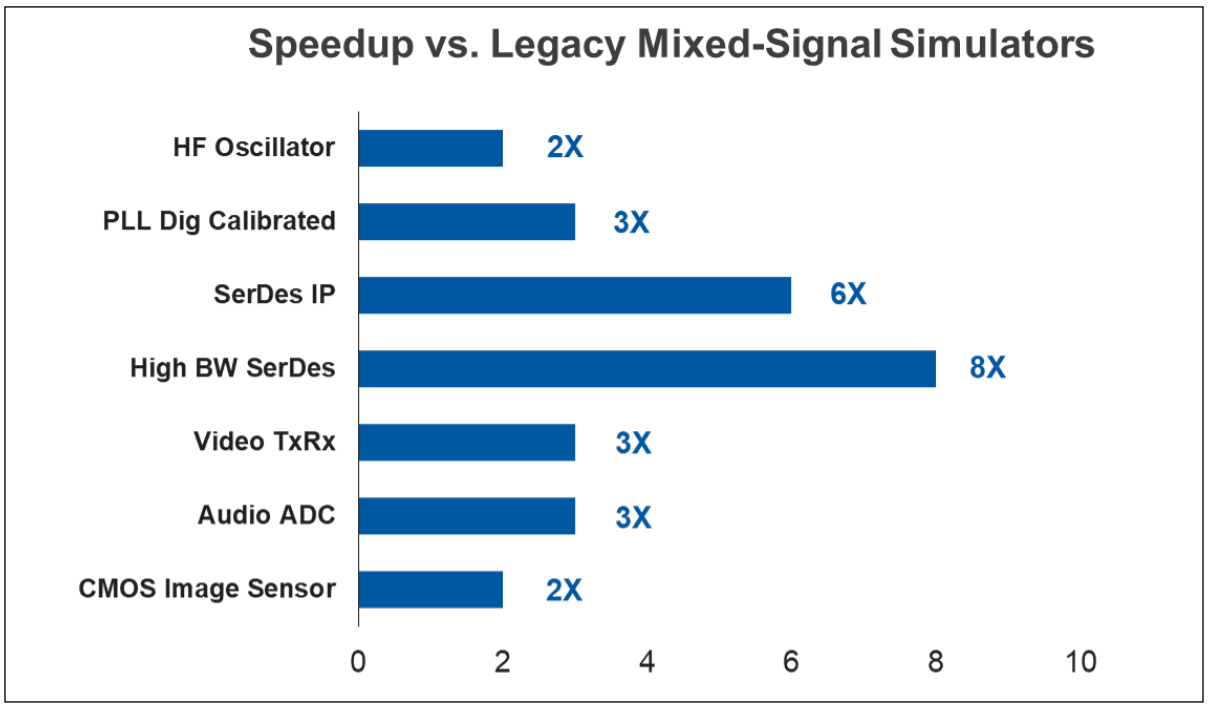

Figure: 7 Symphony speedup versus legacy mixed-signal simulators.

FULLY CONFIGURABLE ARCHITECTURE

Symphony's unique, fully configurable fit-to-purpose architecture (Figure 8) and design aware technologies provide verification teams with the ability to integrate and optimize their mixed-signal flow for any application. Symphony works with all leading digital solvers, including Mentor's Questa®, allowing designers to maximize reuse of their existing verification infrastructure including testbenches, stimuli, scripts, post processing, encrypted IP blocks, and A/D netlists.

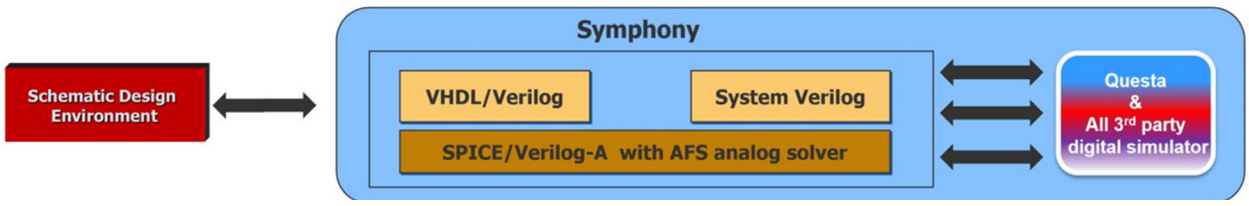

Figure 8: Symphony Configurable Architecture.

BEST IN CLASS USABILITY

Symphony delivers the industry's most intuitive use model with a simple configuration file format and command structure that allows full reuse of existing digital/analog solver command line arguments:

Symphony is also integrated into the leading schematic capture environments and works with both digital and analog centric flows. Symphony offers extensive A/D boundary element (BE) support covering all signal types and multiple power domains, including those with dynamic supplies.

POWERFUL MIXED SIGNAL DEBUG CAPABILITIES

Symphony's state of the art debugging capabilities improve efficiency of design error tracing across A/D interfaces. It offers a powerful debugging cockpit called the BE Browser to give designers the visual BE context needed to trace back design errors to their sources (Figure 9).

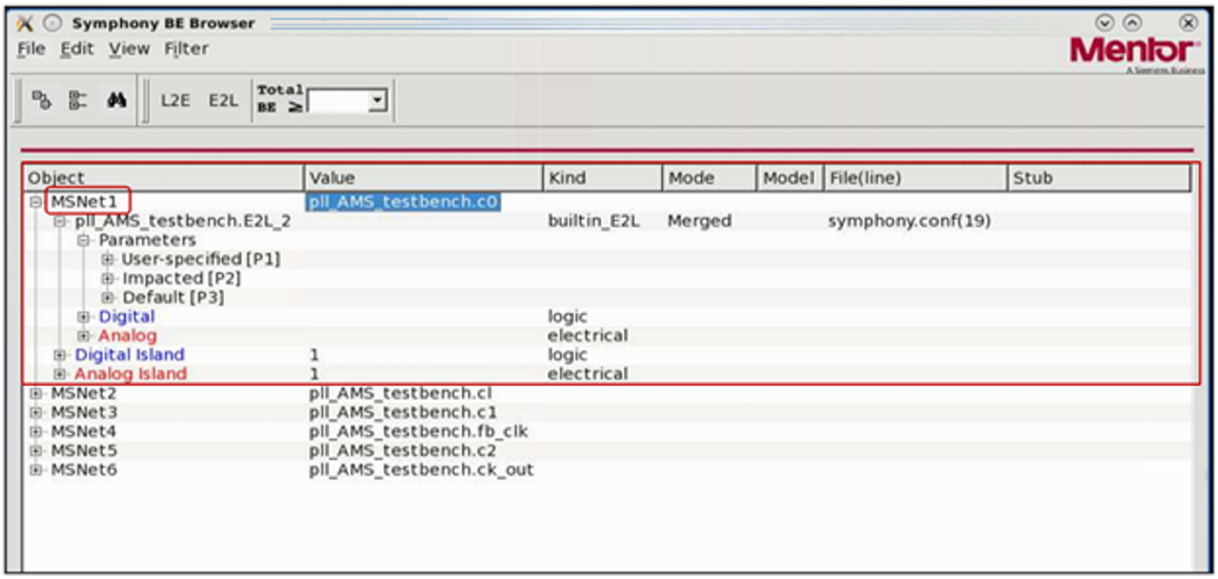

Figure 9: Symphony Boundary Element Browser

Symphony's interactive Tcl mode allows designers to interact dynamically with a running simulation to effectively debug their designs. Interactive Debug leverages interoperability of debug features across the schematic capture tool, waveform viewer, and the simulation kernel to provide a seamless experience.

ADVANCED FEATURES

Symphony offers a powerful set of features designed to increase the verification scope beyond the pure functional realm, into verifying performance aspects of the IC. For example, device noise is critical in nanometer-scale CMOS processes, where it often fundamentally limits circuit performance. Symphony enables gauging the noise impact of analog blocks while preserving the A/D feedback of their parent subsystem, which increases the accuracy of the measurement. Symphony leverages AFS's full-spectrum transient noise analysis capability to accurately predict the device noise impact correlating with 1-2 dB of silicon measurement.

Symphony's Hi-Z checking capability allows designers to detect when a mixed-signal net goes into a 'Z' state, enabling the testbench and the digital control logic to respond correctly to the 'Z' state. Symphony's Save/Restart functionality increases designer productivity for specific applications by reducing full simulation restarts.

CONCLUSION

Verification of mixed-signal IP and SoCs is challenging. As complexity grows, verification engineers cannot rely on the "divide and conquer" approach of verifying digital and analog blocks individually and then stitching them together for full-chip verification. Verification teams need to run an increasing number of mixed-signal simulations at the top level as well as at the subsystem to make sure there are no functional errors due to interactions between analog and digital domains. Even functional errors caused by trivial bugs, such as wrong connectivity, inverted polarity, and incorrect bus order can result in costly silicon re-spins.

While digital verification techniques have evolved over the years, mixed-signal verification is still catching up. Modern analog modeling approaches are developed, but the need for accuracy still takes top priority when it comes to analog verification. Additionally, the analog and digital design environment and verification use models are different and it is challenging to integrate the IC for full mixed-signal verification. To address these challenges, mixed-signal simulation solutions need to be fast, accurate, easy to use, and seamlessly integrate into existing analog and digital verification flows.

Mentor's Symphony Mixed-Signal Platform powered by Mentor's Analog FastSPICE circuit simulator delivers the fastest mixed-signal simulation performance in the industry without sacrificing the analog accuracy needed for verification. Symphony is the industry's most configurable mixed-signal solution that integrates with all the leading digital simulators to allow maximum re-use of verification infrastructure. In addition, Symphony's advance debugging capabilities improve overall mixed-signal verification productivity.

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Trust Tower
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

TFD 3-19 TECH17730-w